ELEG 2904 – DIGITAL DESIGN

Credits and Contact Hours

Four credit hours, 45 hours of instructor contact,

Instructor's Name

Robert Saunders

Textbook

S. Brown and Z. Vranesic, 3rd edition of Fundamentals of Digital Logic with VHDL Design, McGraw-Hill, 2009.

Specific Course Information

a. Catalog Description:
   To introduce students to modern logic concepts, problem solving and design principles, and vocabulary and philosophy of the digital world.
b. Co-requisite: Lab component
c. Required

Specific Goals for the Course

1. Specific outcomes of instructions:
   Upon successful completion of this course, students will understand logic gates, Boolean algebra, combinational logic circuits, and related devices, and will be able to analyze and design arbitrary combinational digital systems and basic sequential circuits. Specifically, students will be able to demonstrate understanding of the following concepts:
   - Number Systems and Digital Arithmetic
   - Logic Gates and Boolean Algebra
   - Combinational Logic Design
   - VHDL
   - CMOS Logic Design
   - Flip-Flops
   - Counters and Registers
   - Mealy and Moore Machine Design and Optimization

2. Indicate the student outcomes listed in Criterion 3 addressed by the course

OUTCOME	HOW IT WAS ADDRESSED
(a)	Students apply mathematics in analyzing digital circuit performance.
(b)	Students implement various digital logic designs and analyze them for timing and function.
(c)	Students implement various digital logic designs to perform functions such as timers and counters.
(e)	Students are required to solve engineering problems related to design and implementation of digital functions

(g)	Students are assigned lab reports
(k)	Students are given lab assignments that require them to implement digital functions using VHDL and implement them in FPGAs.

Lecture Topics:

- Number Systems and Computer Arithmetic (3 classes)
- Boolean Algebra (3 classes)
- Combinational Logic Design (3 classes)
- Digital Hardware (3 classes)
- Introduction to VHDL (3 classes)
- CMOS Logic Design (3 classes)
- Latches and Flip-Flops (3 classes)
- Registers and Counters (3 classes)
- Mealy and Moore Machine Design and Optimization (4 classes)
- Miscellaneous (e.g., ADC, DAC, memory (ROM, EEPROM, SRAM, DRAM), tri-stating) (2 class)

Lab Experiments & Objectives:

- DE2 Board Familiarization: Unsigned and 2^s Complement Addition
- Quartus II and Breadboard Familiarization: Combinational Logic Design using Truth Tables and SSI Implementation
- 7-Segment Display Design and DE2 Implementation
- Combinational Logic Design using K-maps and SSI Implementation
- Combinational Logic Design using Multiplexers and MSI Implementation
- Combinational Logic Design using VHDL and DE2 Implementation
- Stopwatch Design and DE2 Implementation
- Design and Implementation of 2-bit Up/Down Counter using SSI/MSI components and Debounced Switch

Computer Usage

Use of Quartus II to implement lab and homework assignments.

Oral/Written Communications

Students write lab reports for all labs.